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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,082	08/19/2003	Sadayoshi Umeda	107337-00050	3060

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EXAMINER	
HOANG, ANN THI	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,082	UMEDA, SADAYOSHI	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The acronym "LSI" is used but not defined.

Appropriate correction is required.

Claim Objections

1. Claim 1 is objected to because of the following informalities: Line 23 should be changed to "...source-drain path of the transistor." Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art in view of Voldman (US 6,628,159).

Regarding claim 1, the acknowledged prior art of Applicant's disclosure teaches an electrostatic discharge protection circuit (Fig. 3) for protecting an internal circuit 30 of a semiconductor device against an electrostatic discharge, comprising: an internal circuit 30 connected with a first and a second power source terminal VD and VS; a transistor Tr2 with a source and a drain connected to first and second power source terminals VD and VS, respectively; and a voltage-dividing circuit (R2, C3) dividing and supplying the discharge voltages to the gate of transistor Tr2, voltage-dividing circuit

(R2, C3) controlling ON/OFF operation of a source-drain path of transistor Tr2. The acknowledged prior art does not teach that transistor Tr2 switches the source and drain in accordance with a voltage supplied to a back gate, nor does it teach a first diode connected between first power source terminal VD and the back gate or a second diode connected between second power source terminal VS and the back gate.

However, Voldman discloses a transistor 43 switching a source and drain connected to a pad 40 and ground terminal, respectively, a first diode 90 connected between pad 40 and the back gate of transistor 43, first diode 90 supplying a positive discharge voltage generated in pad 40 to the back gate; a second diode 90 connected between the ground terminal and the back gate, second diode 90 supplying a positive discharge voltage generated in the ground terminal to the back gate. See Fig. 9. Transistor 43 is a pass transistor in a protection circuit against ESD events and voltage surges. First and second diodes 90 are disclosed to be part of a circuit control network that controls the voltage of the body of transistor 43 and provides overvoltage protection to transistor 43. From Fig. 9, it can be seen that a positive discharge voltage generated in pad 40 would be supplied to the back gate of transistor 43 through first diode 90. It can also be seen that a positive discharge voltage generated in the ground terminal could be supplied to the back gate via second diode 90 by simply switching the direction of second diode 90 so that the cathode is connected to the back gate and the anode to the ground terminal, since it is well known in the art that a diode can be used to allow unidirectional flow current based on its orientation. Transistor 43 acts as a switch, wherein the source and drain are interchangeable. The voltage supplied to the back

gate, in reference to the potentials of the other terminals of transistor 43 (specifically, which is more positive), determines which terminal of transistor 43 serves as the source and which terminal serves as the drain (in other words, the direction of current flow through transistor 43). Therefore, transistor 43 switches the source and drain in accordance with the voltage supplied to the back gate. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the first diode of Voldman between the first power source terminal and back gate of the acknowledged prior art and the second diode of Voldman between the second power source terminal and back gate of the acknowledged prior art in order to have an ESD protection circuit which provides ESD protection to the internal circuit and further provides overvoltage protection to the pass transistor.

Regarding claim 2, in the combination of the acknowledged prior art and Voldman, (see above rejection), transistor Tr2 comprises a first power source terminal side serving as a source when the positive discharge voltage is supplied from the first power source terminal VD to the back gate, and a second power source terminal side serving as a source when the positive discharge voltage is supplied from the second power source terminal VS to the back gate. With diodes 90 connected between the first and second power source terminals VD and VS, respectively, and the back gate of transistor Tr2, a positive discharge voltage generated in the first power source terminal VD is applied to the back gate and a current flows from the first power source terminal side of transistor Tr2 to the second power source terminal side. Accordingly, when the cathode of second diode 90 is positioned to be connected to the back gate, a positive

discharge voltage generated in the second power source terminal VS is applied to the back gate, resulting in a current flowing from the second power source terminal side to the first power source terminal side.

Regarding claim 5, the acknowledged prior art teaches diodes (D7, D8) connected between an input/output terminal V of internal circuit 10 and first and second power source terminals VD and VS, respectively, diodes (D7, D8) carrying the discharge voltage produced in input/output terminal V to first and the second power source terminals VD and VS, respectively, in the form of an electric current.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art in view of Voldman (US 6,628,159) as applied to claim 1 above, and further in view of Krzentz (US 5,796,296). The acknowledged prior art teaches a voltage-dividing circuit (R2, C3) that divides the discharge voltage and supplies the voltage to the gate of transistor Tr2. Voldman also discloses a voltage-dividing circuit (41, 71) performing the same function (see Fig. 9). Neither the acknowledged prior art nor Voldman teach the discharge voltage being equally divided.

However, Krzentz teaches a two-to-one voltage-divider wherein the output voltage is one half of the input voltage. See all figures and column 2, lines 22-37. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the two-to-one voltage divider of Krzentz in the electrostatic discharge protection circuit of the acknowledged prior art in order to equally divide the discharge voltage. Equal voltage division would serve as a control method to keep the gate of the transistor indiscriminate between a discharge voltage supplied by the first power source terminal

and that supplied by the second power source terminal, therefore allowing consistent operation of the transistor even as the source and drain were switched.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art in view of Voldman (US 6,628,159) as applied to claim 1 above, and further in view of Zhou (US 5,446,644). Neither the acknowledged prior art nor Voldman teach a voltage-dividing circuit that unidirectionally runs a current caused by the discharge voltage.

However, Zhou discloses a voltage-divider for unidirectional transmission that divides a high voltage input into a low voltage DC output (see Fig. 1 and abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the unidirectional voltage-divider of Zhou in the electrostatic discharge protection circuit of the acknowledged prior art in order to divide a high discharge voltage input into a low voltage output for the gate of the transistor.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang (US 6,385,116) teaches an ESD protection circuit for a semiconductor integrated device comprising an internal circuit connected with a power source line and ground line; a first and second diode connected between an input/output terminal of the internal circuit and the power source line and ground line, respectively, the first and second diode passing discharge current produced in the input/output terminal to the power source line and ground line, respectively; and a

charge pass circuit for flowing discharge current between the power source line and ground line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Mondays through Fridays, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ATH

PHUONG T. VU
PRIMARY EXAMINER